IN THE SPECIFICATION

Please replace the following paragraphs as indicated below:

[0018] FIG. 1 depicts a schematic diagram of a semiconductor wafer processing system 100 that may illustratively be used to practice the invention. One processing system suitable for practicing the invention is a TRANSFORMA™ processing system, available from Applied Materials, Inc. of Santa Clara, Calif. A similar processing system is disclosed in commonly assigned U.S. Pat. No. 6,486,492 B1, issued Nov. 26, 2002, as well as U.S. Pat. No. ~~6,150,664~~ 6,150,664, issued Nov. 21, 2000, which are incorporated herein by reference. Herein the particular embodiment of the system 100 is provided for illustrative purposes and should not be used to limit the scope of the invention.

[0040] Referring to FIG. 3A, at step 202, a substrate 300 (e.g., silicon (Si) wafer, and the like) is transported to the metrology module 126 of the processing system 100. The substrate 300 generally comprises regions 332 and regions 334 (both regions are depicted using broken lines) where the sources and drains will be formed using an ion implant process after fabrication of the gate structure is completed, a film stack 302 for forming a gate structure of the transistor being fabricated, and a patterned mask 314. The source and drain regions 332, 334 are separated by a channel region 336 in each of the transistors being manufactured. In one embodiment, the film stack 302 comprises a gate dielectric layer 304, a gate electrode layer 306, and a gate conductor layer 308. The patterned mask 314 protects region 320 above the channel region 336 and portions of the ~~wells~~ regions 332 and 334, and exposes adjacent regions 321 and 322 of the substrate 300.

[0054] In FIG. 4A, a graph 400 depicts an exemplary pre-etch statistical distribution 418 ~~(y-axis 402)~~ of the width 303 of the patterned masks 314 for substrates 300 of a batch of the substrates. The distribution 418 is plotted with respect to an x-axis 404,

representing the width of the CD, and a y-axis 402, representing the number of substrates. The distribution 418 [[402]] has a width 416 (e.g., 6σ, or about 99.5% of the substrates), where a center 410 of the distribution relates to the nominal value of the width 303 of the patterned masks 314. Boundaries 412 and 414 for the distribution 418 [[402]] illustratively correspond to the minimal and maximal values for the width 303 on the substrates 300 and limit the distribution to a +/- 3σ range around the center 410, respectively. A portion 406 of the distribution 418 [[402]] above the centerline 411 relates to the substrates 300 having widths 314 that are greater than the nominal width 416. Accordingly, a portion 408 of the distribution 418 [[400]] below the centerline 411 relates to the substrates 300 having widths 314 that are smaller than the nominal width 410. In one exemplary embodiment, the values 416, 410, 412, and 414 were 20, 90, 80, and 100 nm, respectively.

[0055] In FIG. 4B, a graph 420 depicts an exemplary post-etch statistical distribution 428 [[422]] of the width 305 of the gate conductor layer 308 of the substrates 300 of the same batch of the substrates after the adjusted etch process of 208. The distribution 420 is plotted with respect to an x-axis 424, representing the width of the CD, and a y-axis 422, representing the number of substrates. The distribution 428 [[422]] has a width 426 (e.g., 6σ, or about 99.5% of the substrates), where a center 430 of the distribution relates to the nominal value of the width 305 of the gate conductor layer 308. Boundaries 432 and 434 of the distribution 428 [[422]] illustratively correspond to the minimal and maximal values of the width 305 for the substrates 300 and limit the distribution to a +/- 3σ range around the center 430, respectively. In one exemplary embodiment, the values 426, 430, 432, and 434 were 5, 90, 87.5, and 92.5 nm, respectively.

[0056] As such, the inventive method produced etched structures in the gate conductor layer 308 which have approximately 4 times narrower post-etch statistical distribution 428 [[422]] for the critical dimensions (i.e., width 305) than the pre-etch statistical distribution 418 [[402]] for the critical dimensions (i.e., width 303) of the

respective elements of the patterned etch mask 314. Additionally, the statistical distribution for the post-etch width 309 of the patterned etch mask 314 is similarly narrowed.

[0058] The duration of the overetch period is expressed using units for deviation of the width 303 from the nominal value 410 (discussed in reference to FIG. 4A above). More specifically, a nominal duration 510 of the second period relates to the patterned mask 314 having the nominal value 410 (i.e., when the deviation of the width 303 is equal to 0). In FIG. 5, the portions 508 and 506 of the graph 500 relate to the portions 408 and 406 in the graph 400 ~~402~~ (FIG. 4A), respectively. Accordingly, durations 510, 512, and 514 of the overetch period correspond to the patterned masks 314 having, respectively, values 410, 412, and 414 for the width 303. Using the graph 500, a duration 520 for the overetch period that corresponds to the patterned mask 314 having a deviation 518 from the nominal width 410 may be defined as shown with arrow 522.